Three-Dimensional Millimeter-Wave Photonic Integrated Circuits on Si

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Abstract — **We have demonstrated two millimeter-wave photonic integrated circuits: a coplanar waveguide (CPW) and a patch antenna, each of which is monolithically integrated with a high-speed InP/InGaAs photodiode on Si substrate. The passive elements are made on a thick low-k interlayer dielectric which makes the attenuation of the CPW much lower than that for a CPW on Si and constant from DC to 100 GHz. Furthermore, we optimized the via geometry to maintain signal waveform integrity. For the patch antenna, we demonstrated the radiation of millimeter-wave signal with power of over 0.1 mW at 120 GHz.**

I. INOTRODUCTION

The significant advances made in Si technology over the past several decades have enabled ultralarge scale integrated circuits (ULSIs). The speed of Si-based devices is increasing, and Si ULSIs make it possible to perform complicated digital signal processing. In such applications as fiber optic communications, optical interconnections, wireless communications and sensing, Si devices are on the verge of being combined with ultrahigh-speed optical and electrical devices made of III-V compound semiconductors to achieve higher functionality, lower cost and higher performance [1] [2]. This wave of technological fusion is also sweeping over millimeter-wave photonics [3]. In addition, Si substrate is advantageous for heat dissipation and handling in fabrication and packaging because Si has higher thermal conductivity and mechanical strength than compound semiconductors.

In this paper, we present a millimeter-wave photonic integrated circuit (MWP-IC) technology on Si substrate, which can be applied to millimeter-wave broadband communications and measurement systems. In such circuits, Si devices and III-V-based electrical and optical devices are substrate and three-dimensionally (3-D) integrated with passive components. To make the MWP-ICs a reality, as the first step, we have developed millimeter-wave coplanar waveguides (CPWs) and patch antennas each integrated with a photodiode on Si substrate. The former can be used for millimeter-wave signal transmission on a chip and the latter for millimeter-wave wireless interface outside a chip. For these circuits, we took advantage of recently developed high-output high-speed InP/InGaAs uni-traveling-carrier photodiodes (UTC-PDs) [4]. Here, we describe the structure, design methods, and fabrication of the ICs, and present their performance and characteristics.

II. STRUCTURE OF 3-D MWP-ICS

The structure of a MWP-IC is illustrated in Fig. 1. Si devices are integrated with heterogeneous material devices, including photonic and electrical devices, close to Si substrate. Optical waveguides are embedded in the interlayer dielectric. Passive components, such as

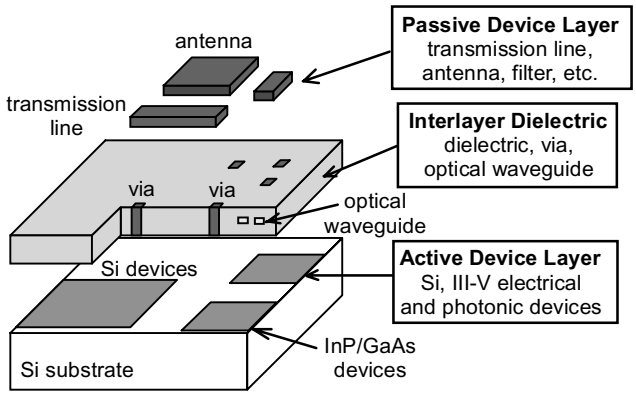

Fig. 1. Conceptual schematic of a millimeter-wave photonic integrated circuit.

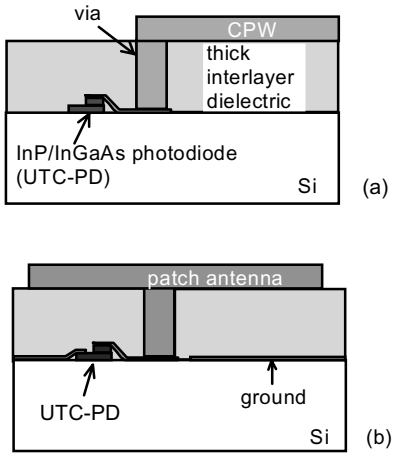

Fig. 2. Schematic cross-sectional drawing of (a) CPW and (b) patch antenna integrated with UTC-PDs on Si substrate.

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transmission lines, filters, and antennas, are made on a thick low-k interlayer dielectric and connected with active devices close to Si substrate by vias embedded in the thick interlayer dielectric.

Two examples of MWP-ICs presented in this paper, CPW and antenna, are illustrated in Figs. 2 (a) and (b), respectively. As mentioned above, each passive element is made on a thick low-k interlayer dielectric and connected with a UTC-PD on Si substrate by Au vias. In order to reduce conductor loss, the CPW and patch antenna are made of thick Au. For the CPW, the loss due to the high permittivity and conductivity of the Si can be reduced by separating the CPW from Si. For the patch antenna, this technology allows us to fabricate the antenna and circuit ground on the same side of substrate, which eliminates vias through substrate and complicated backside process. Moreover, this structure provides for the reduction of the Q factor of the antenna, broadening the bandwidth, and improving the radiation efficiency.

III. Design of CPWs

In the 3-D interconnection shown in Fig. 2 (a), long vias may cause waveform distortion due to such parasitic effects as reflections and resonances in the via region. In order to prevent such a waveform distortion, we investigated the effect of the via geometry on waveform using a 3-D electromagnetic simulator based on the finite-difference time-domain (FDTD) method. In the simulation, a pulse signal was generated at the UTC-PD location, and waveforms of pulses passing through the via and propagating in the CPW were calculated. The simulated structures consisted of one thin and four 10-μm thick layers, consistent with our fabrication process.

The effect on the waveform by the via geometry in planes perpendicular (x-y) and parallel (y-z) to the propagation (z) direction was investigated. We found that, in y-z plane, gradually sloping transition mitigates waveform distortion. The via geometry in x-y plane is also important. In our method to minimize waveform distortion, each via layer is assumed to be a CPW and the ground-signal spacing is chosen to make the characteristic impedance 50 Ω for that CPW. So, the ground vias in x-y plane are also sloped.

Figures 3 (a), (b), and (c) illustrate abrupt transition via, sloping transition via in only x-y plane, and sloping transition via in both x-y and y-z planes, respectively. The effect of the via geometry can be seen by comparing the simulation result for the sloping transition via in both planes with those for the sloping transition via in only x-y plane and the abrupt transition via. These simulation results are shown in Fig. 3 (d). In top waveform of this figure, which corresponds to the abrupt transition via, there is an oscillation after the main peak. In contrast, the amplitude of oscillation in middle waveform for the sloping transition via in x-y plane is smaller. In bottom waveform for the sloping transition via in both planes, the oscillation almost vanishes.

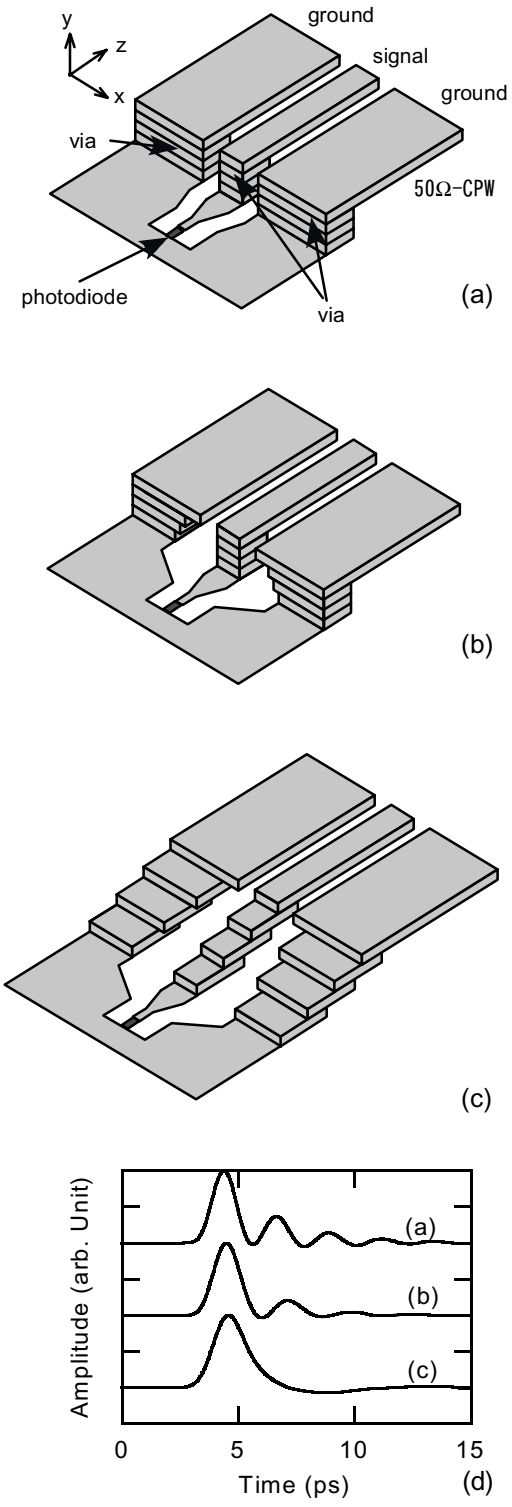

Fig. 3. Schematic drawings of the CPWs with (a) the abrupt transition via and sloping transition vias (b) in x-y plane and (c) in both x-y and y-z planes, along with (d) the simulation results.

IV. Fabrication of ICs

The circuits were made on 2-inch high resistivity (3 kΩ cm) Si wafers. The UTC-PDs were fabricated on a Si substrate by using full-wafer wafer bonding which allows us to perform the whole process, including four-layer interconnection stack, on a full wafer. After removing the InP substrate, a conventional UTC-PD process was carried out [5].

Next, 10-μm-thick Au CPWs and patch antennas were fabricated on 30-μm-thick interlayer dielectric. Polybenzoxazole (PBO) was used for the interlayer dielectric. PBO used in our fabrication has low dielectric constant (low-k of 2.9) and positive photosensitivity. The CPWs and patch antennas on the PBO were connected to the pad of the UTC-PD by Au vias embedded in the PBO. This was accomplished by using a three-level damascene process. The damascene process starts with photolithographic patterning of 10-μm thick PBO to form via holes. The via holes are then filled with Au by selective electroplating. In the selective electroplating, conventional resist covers the whole wafer except the via holes so that Au is only deposited in the via holes. The surface is planarized by chemical-mechanical polishing.

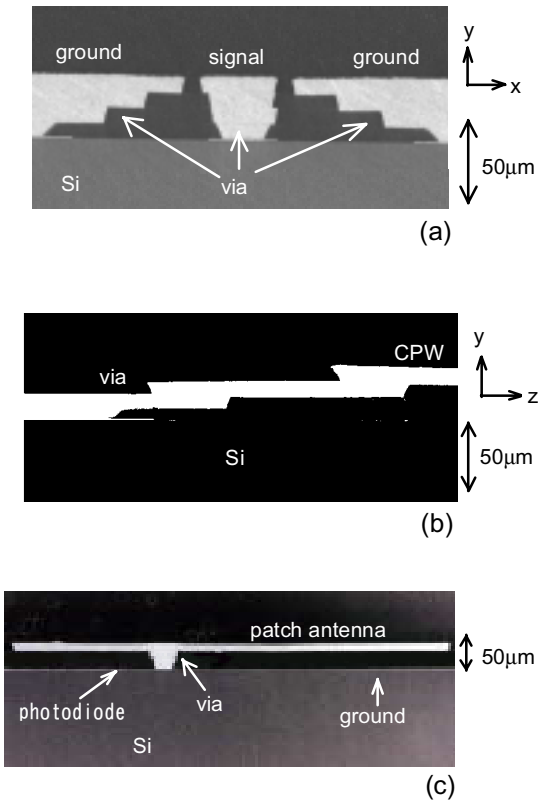

Fig. 4. Cross-sectional SEM images of the CPWs with the sloping transition via (a) in x-y plane and (b) in both x-y and y-z planes, and (c) patch antenna.

After forming a 30-μm-thick PBO interlayer dielectric and Au vias, the CPWs and patch antennas are formed by the fourth selective electroplating.

Figure 4 shows cross-sectional SEM images of the CPW and patch antenna. In fabrication, the actual shapes of the via, CPW, and antenna metal in cross section depend on the shapes of the PBO and resist used in selective electroplating. Because PBO and resist have a tilted walls, the via, CPW, and antenna metal have an overhang structure. The tilted-wall PBO allows us to deposit uninterrupted seed layer for electroplating.

V. Results and Discussion

For this paper, we fabricated and measured CPWs on PBO with two types of vias, as well as CPWs placed on Si substrate. This allows us to confirm the superior characteristics of the CPWs on the thick dielectric and verify the via design.

In the measurement, an electrical pulse was generated

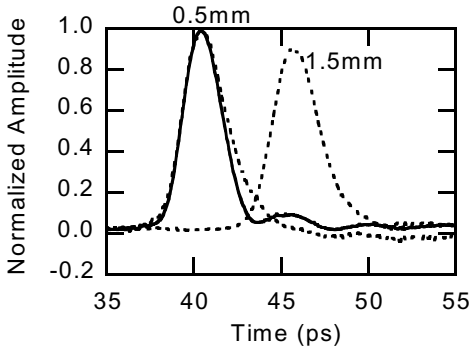

Fig. 5. Measured waveforms of an electrical pulse propagating along the CPW. The solid and dashed lines correspond to the results for the CPWs with the sloping transition in x-y plane and in both x-y and y-z planes, respectively.

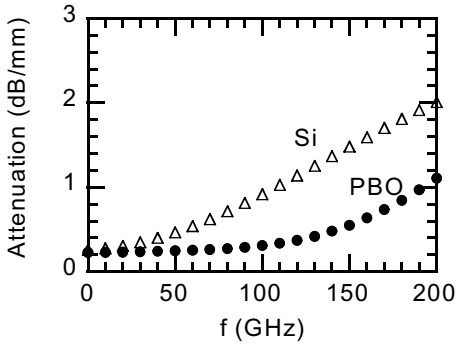

Fig. 6. Frequency dependence of the attenuation for CPWs on PBO (circles) and directly on Si (triangles).

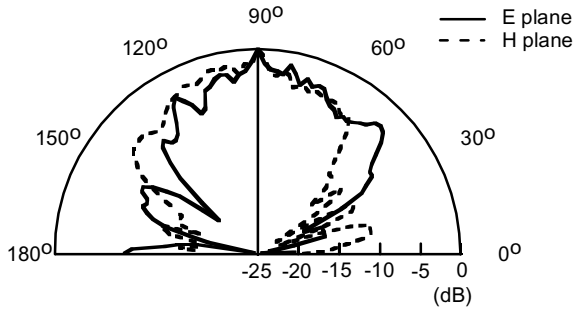

Fig. 7. Measured E- and H-plane patterns of packaged patch antenna integrated with UTC-PD.

from the UTC-PD by injecting a 1.55-μm wavelength 500-fs-wide optical pulse. The waveform of the electrical pulse propagating along the CPW was measured at various distances from the device by an electro-optic sampling (EOS) technique [6]. The UTC-PDs on Si exhibited a similar performance to ones on InP. Electrical pulses entering CPW in our measurement had the pulse peak of 0.7 V and the pulse width of 2.6 ps, which corresponds to 3-dB bandwidth of over 100 GHz. Thus, integrating UTC-PDs with millimeter-wave devices is not only useful for the final MWP-ICs, but is an excellent way to characterize these components during the design stage.

Figure 5 shows the electrical pulse waveforms measured at 0.5 mm and 1.5 mm from the device. The solid and dashed lines represent the waveforms for the CPWs with the sloping transition in x-y plane and in both x-y and y-z planes, respectively. While there was an oscillation in the waveform for the CPW with the sloping transition in x-y plane, the oscillation nearly vanished in the waveform for the CPW with the sloping transition in both x-y and y-z planes. This is qualitatively in agreement with the simulation results. The quantitative discrepancy in the oscillation amplitude was probably caused by the difference between the shapes of the via in the simulation and the fabricated samples.

Figure 6 compares the attenuation frequency dependences of CPWs fabricated on PBO and Si substrate. CPW on Si substrate is also made of 10-μm thick Au. The attenuation for the CPW on 30-μm-thick PBO is constant up to 100 GHz and the magnitude of the attenuation is much lower than that for the CPW on Si. Attenuation of the CPW on Si is expected to be even higher if they were made on low resistivity Si, normally used for ULSI. This indicates that separating the CPW from the Si is effective for reducing transmission loss.

For the patch antenna integrated with the UTC-PD, we measured the radiation of millimeter-wave signal at 120 GHz. The millimeter-wave was generated by the illumination of the UTC-PD with a 120-GHz sinusoidal optical signal. The power radiated from the patch antenna was detected by a Shottky-barrier diode mounted on a Horn antenna. Figure 7 shows the measured E- and H-plane patterns. The maximum detected radiation power exceeded 0.1 mW. This is the first demonstration of monolithically integrated photonic emitter operating at frequencies above 100 GHz.

VI. Conclusion

We demonstrated novel millimeter-wave CPW and patch antenna, each of which was integrated with a high-speed InP/InGaAs photodiode on Si substrate. These circuits were fabricated by using wafer bonding and four-layer thick metal/dielectric interconnection stack. For the CPWs, this technology makes the attenuation much lower than that of the CPWs on Si substrate and constant up to 100 GHz. Furthermore, optimizing via geometry eliminates waveform distortion. For the patch antenna, this fabrication technology enables the antenna to have broadband and high radiation efficiency.

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References

[1] N. M. Jokerst. M. A. Brooke, O. Vendier, S. Wilkinson, S. Fike, M. Lee, E. Twyford, C. Brent, B. Buchanan, and S. Wills, "Thin-film multimaterial optoelectronic integrated circuits", IEEE Trans. Comp. Packag. Manufact. Technol. B, Vol. 19, No. 1, pp. 97-106, 1996.

[2] H. Wada and T. Kamijoh, "Wafer bonding of InP to Si and its application to optical devices", Jpn. Appl. Phys., Vol. 37, pp. 1383-1390, 1998.

[3] T. Nagatsuma, K. Machida, H. Ishii, N. Sahri, M. Shinagawa, H. Kyuragi, and J. Yamada, "Innovative integration based on silicon-core technologies for sensor and communications applications", International Journal of High Speed Electronics and Systems, Vol. 10, No. 1, pp. 205-215, 2000.

[4] T. Ishibashi, T. Furuta, H. Fushimi, S. Kodama, H. Ito, T. Nagatsuma, N. shimizu, and Y. Miyamoto, "InP/InGaAs uni-traveling-carrer photodiodes", IEICE Trans. Electron., Vol. E83-C, pp. 938-949, 2000.

[5] Y. Royter, T. Furuta, S. Kodama, N. Sahri, T. Nagatsuma, and T. Ishibashi, "Integrated packaging of uni-traveling-carrier photodiodes on sapphire substrate by wafer bonding", Terahertz and Gigahertz Photonics, Proceeding of SPIE, Vol. 3795, pp. 619-630, 1999.

[6] N. Sahri, T. Nagatsuma, K. Machida, H. Ishii, and H. Kyuragi, "Characterization of micromachined coplanar waveguides on silicon up to 300 GHz", 29th European Microwave Conference, pp. 254-257, 1999.